

FIG. 1

108290" 50246860

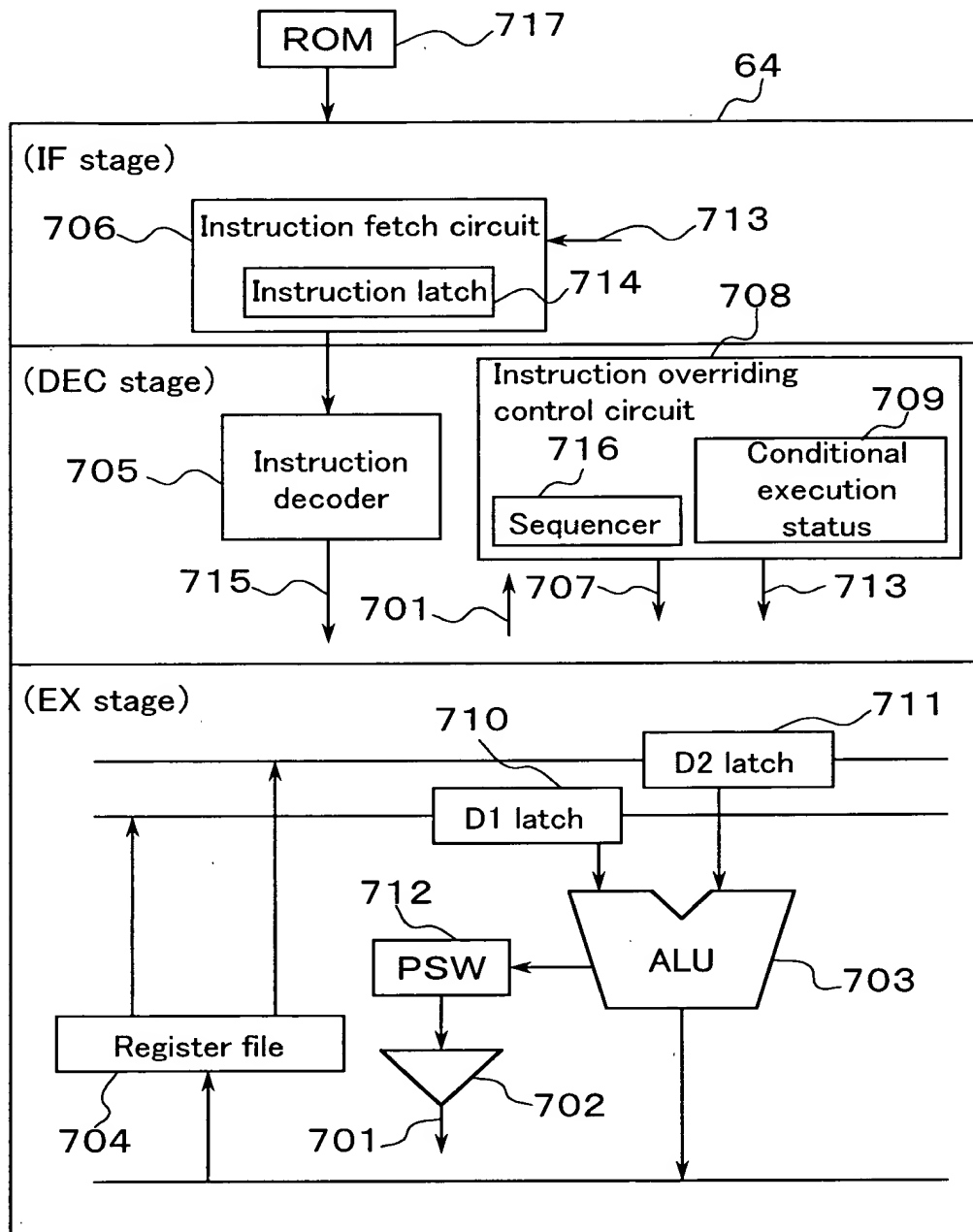


FIG. 2

0964205-062801

1082290-50246860

Exclusive condition \ Conditional execution status	x'00	x'01	x'10	x'11
1	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 3A

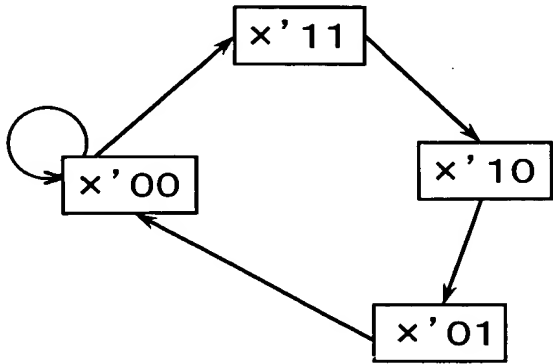


FIG. 3B

IF stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
DEC stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
EX stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6

Conditional execution status	x'00	x'00	x'11	x'10	x'01	x'00	x'00
Exclusive condition	0	0	0	1	1	1	0
Instruction overriding signal	0	0	0	0	1	0	0
	t1	t2	t3	t4	t5	t6	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	[t61 t62]	

FIG. 4

First line	SUBIFEZF R0,R1
Second line	MOV R2,R4
Third line	MOV R3,R4
Fourth line	ADD R5,R6
Fifth line	NOP
Sixth line	NOP

FIG. 5

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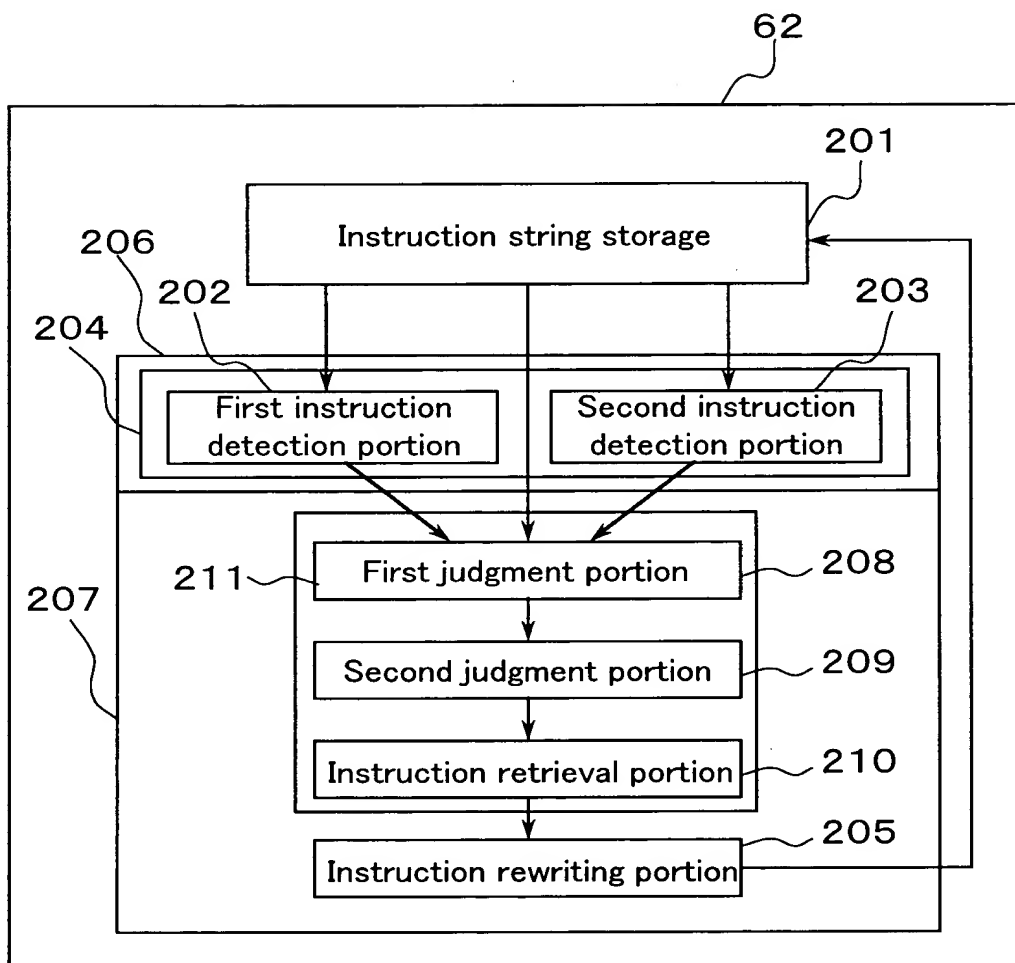


FIG. 6

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First line	ADD R5,R1
Second line	SUB R0,R1
Third line	MOVIFZF R2,R4
Fourth line	MOVIFNZF R3,R4
Fifth line	ADD R4,R5
Sixth line	MOV R5,R7
Seventh line	MOVIFZF x'0001,R6
Eighth line	MOV R6,R0

FIG. 7

First line	ADD R5,R1
Second line	SUBIFEZF R0,R1
Third line	MOV R2,R4
Fourth line	MOV R3,R4
Fifth line	ADD R4,R5
Sixth line	MOV R5,R7
Seventh line	MOVIFZF x'0001,R6
Eighth line	MOV R6,R0

FIG. 8

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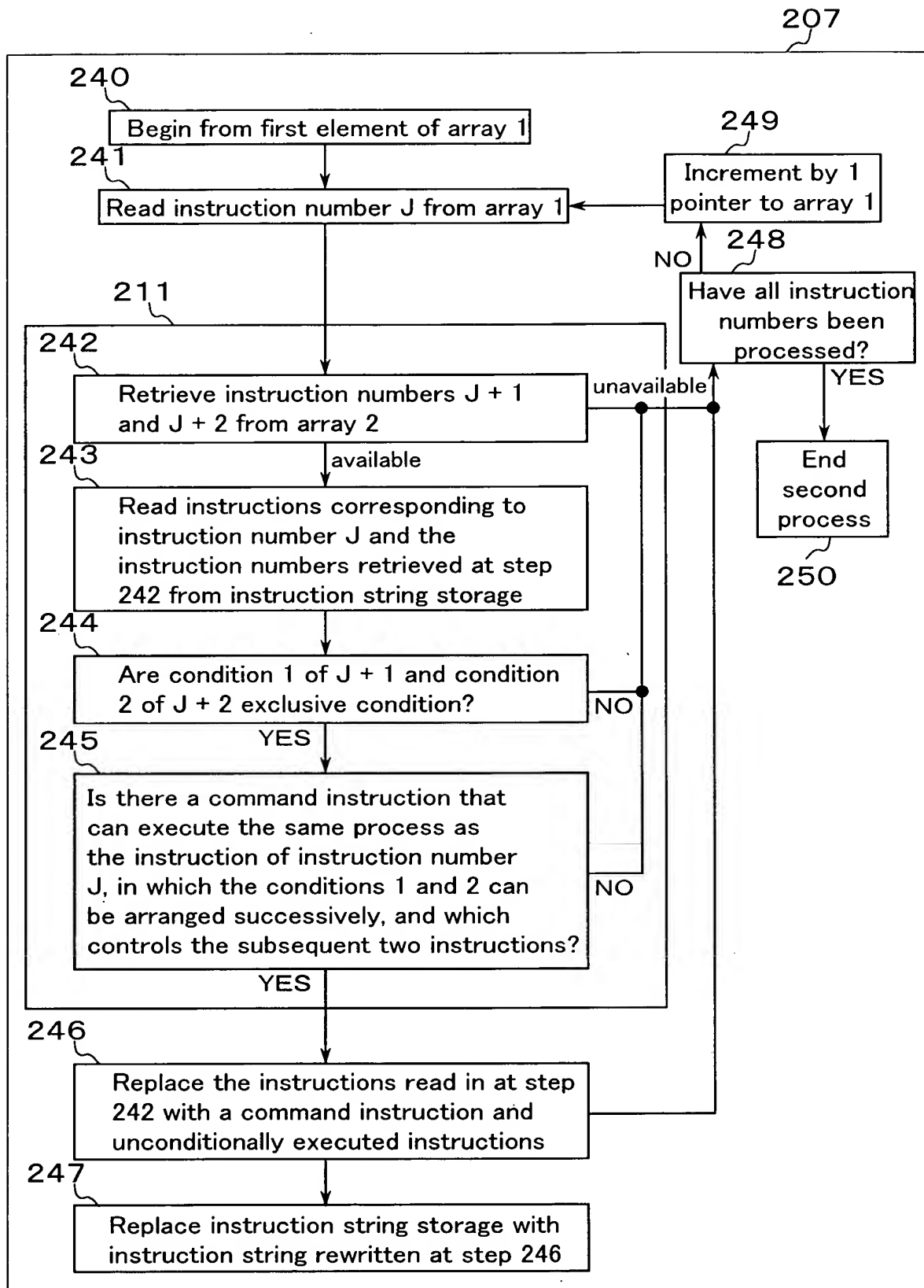


FIG. 10

Exclusive condition	Conditional execution status				
		x'000	x'010 or x'001	x'100 or x'011	x'101
1		Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"	Instruction overriding signal "0"
0		Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 11A

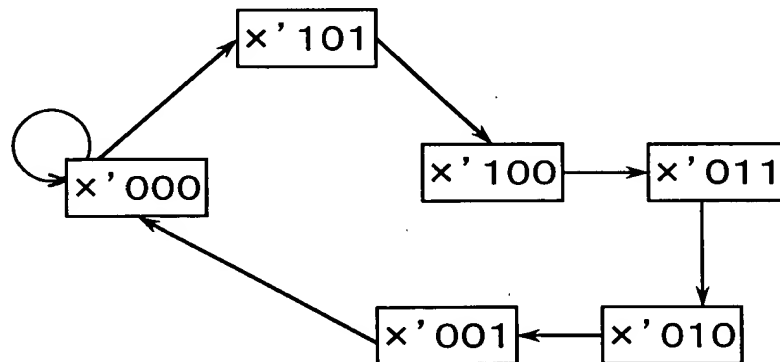


FIG. 11B

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First line	SUBIFEXZF R0,R1
Second line	MOV R2,R6
Third line	MOV R3,R7
Fourth line	MOV R4,R6
Fifth line	MOV R5,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 12

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FIG. 12

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7	Instruction 8
DEC stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7
EX stage		Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7

Conditional execution status	x'000	x'000	x'101	x'100	x'011	x'010	x'001	x'000	x'000
Exclusive condition	0	0	0	1	1	1	1	1	1
Instruction overriding signal	0	0	0	0	0	1	1	0	0
	t1	t2	t3	t4	t5	t6	t7	t8	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	[t61 t62]	[t71 t72]	[t81 t82]	

FIG. 13

First line	SUB R0,R1
Second line	MOVIFZF R2,R6
Third line	MOVIFZF R3,R7
Fourth line	MOVIFNZF R4,R6
Fifth line	MOVIFNZF R5,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 14

First line	SUB R0,R1
Second line	MOVIFZF R2,R6
Third line	MOVIFNZF R4,R6
Fourth line	MOVIFNZF R5,R7
Fifth line	MOVIFZF R3,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 15

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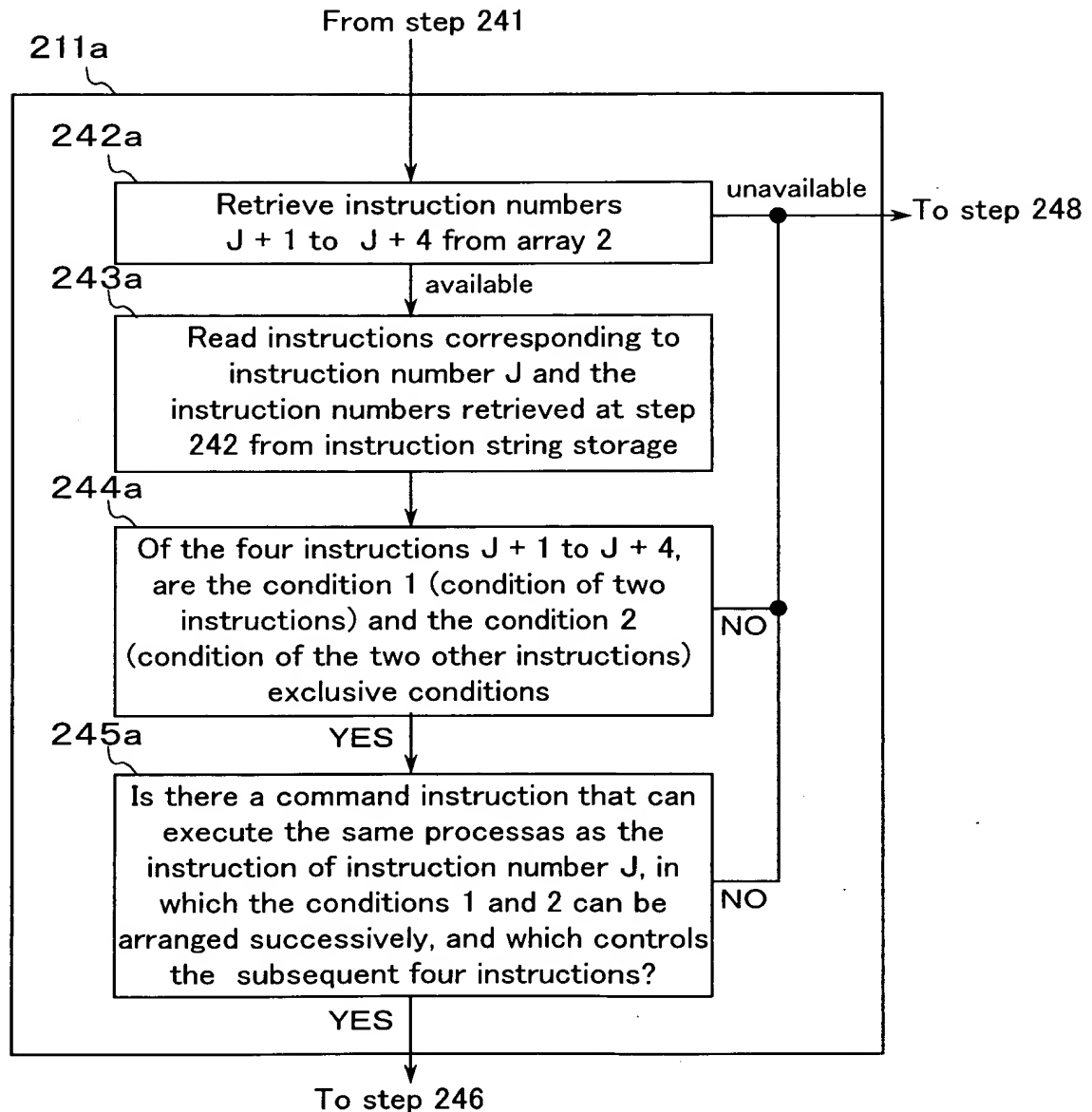


FIG. 16

Exclusive condition	Conditional execution status	x' 00	x' 01	x' 10
1		Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"
0		Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"

FIG. 17A

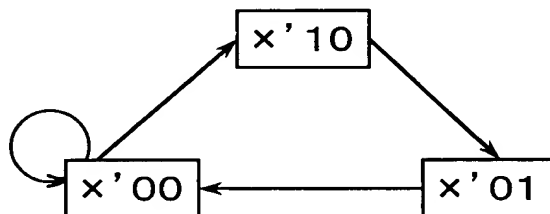


FIG. 17B

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First line	SUBIFXZF R0,R1
Second line	MOV R2,R3
Third line	ADD R3,R6
Fourth line	MOV R4,R7

FIG. 18

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IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5
DEC stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4
EX stage			Instruction 1	<del>Instruction 2</del>	Instruction 3

Conditional execution status	x'00	x'00	x'10	x'01	x'00	x'00
Exclusive condition	0	0	0	1	1	1
Instruction overriding signal	0	0	0	1	0	0
	t1	t2	t3	t4	t5	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	

FIG. 19

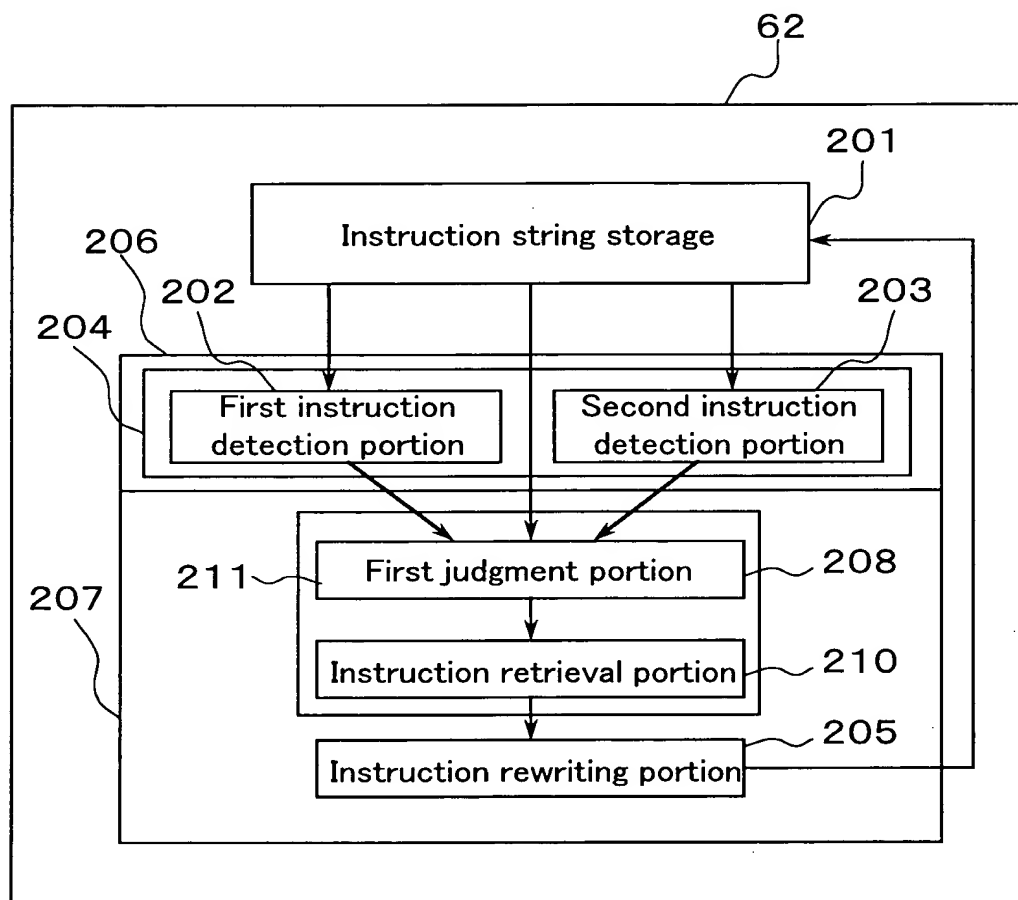


FIG. 20

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First line	SUB R0,R1
Second line	MOVIFNZF R2,R3
Third line	ADD R3,R6
Fourth line	MOV R4,R7

FIG. 21

TOP SECRET

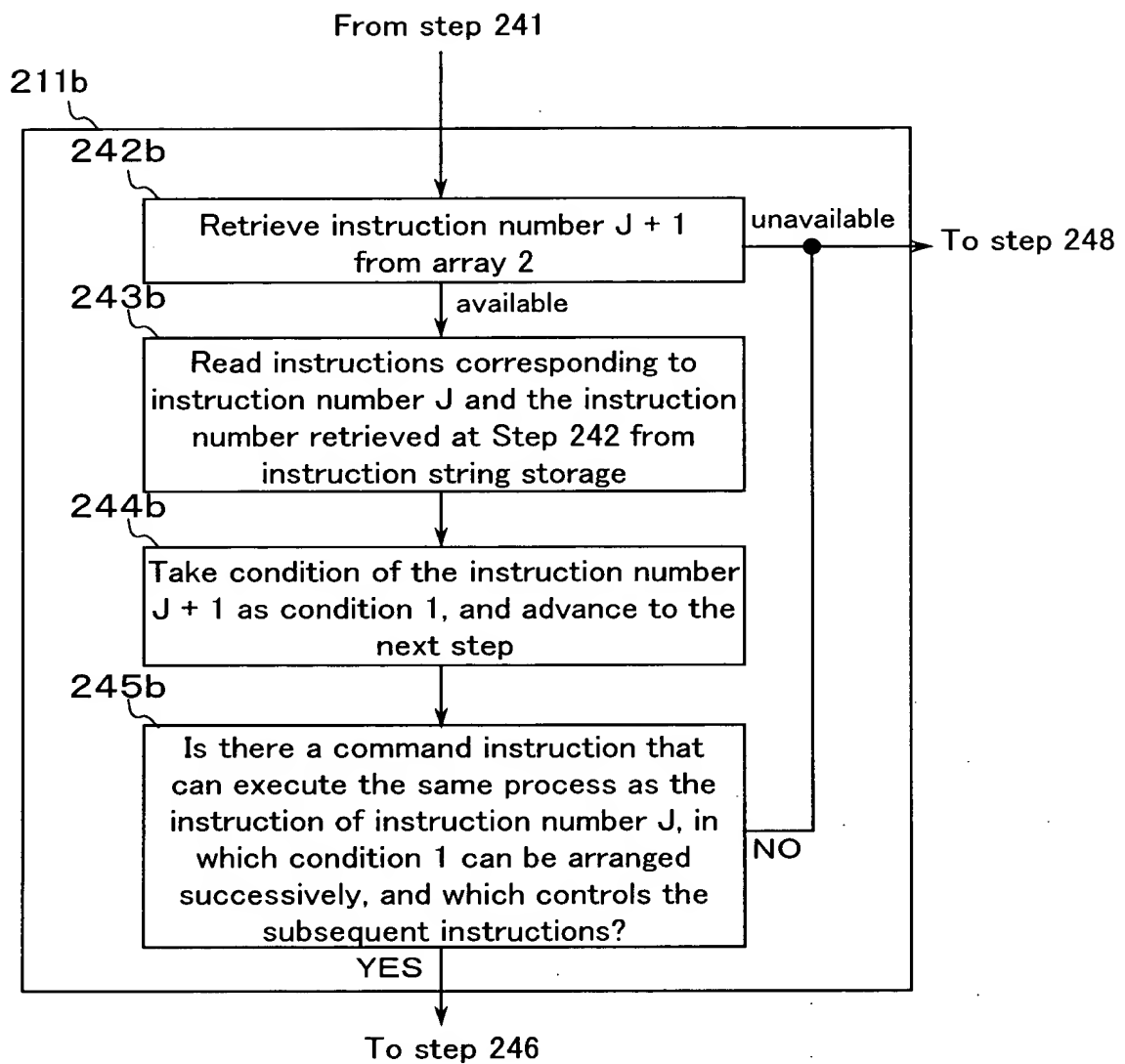


FIG. 22

Exclusive condition	Conditional execution status	x' 00	x' 01	x' 10	x' 11
1		Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "1"	Instruction overriding signal "0"
0		Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"

FIG. 23A

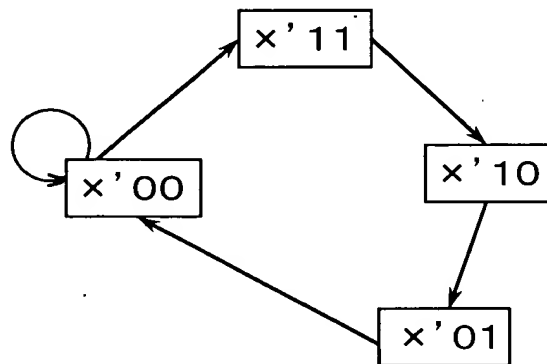




FIG. 23B

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First line	SUBIFNXZF R0,R1
Second line	MOV R2,R3
Third line	MOV R5,R4
Fourth line	ADD R3,R6
Fifth LINE	MOV R4,R7

FIG. 24

108290-50246360

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
DEC stage	Instruction 1		Instruction 2	Instruction 3	Instruction 4	Instruction 5
EX stage			Instruction 1			Instruction 4

Conditional execution status	x'00	x'00	x'11	x'10	x'01	x'00	x'00
Exclusive condition	0	0	0	1	1	1	1
Instruction overriding signal	0	0	0	1	1	0	0
	t1	t2	t3	t4	t5	t6	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	[t61 t62]	

FIG. 25

First line	SUB R0,R1
Second line	MOVIFNZF R2,R3
Third line	MOVIFNZF R5,R4
Fourth line	ADD R3,R6
Fifth line	MOV R4,R7

FIG. 26

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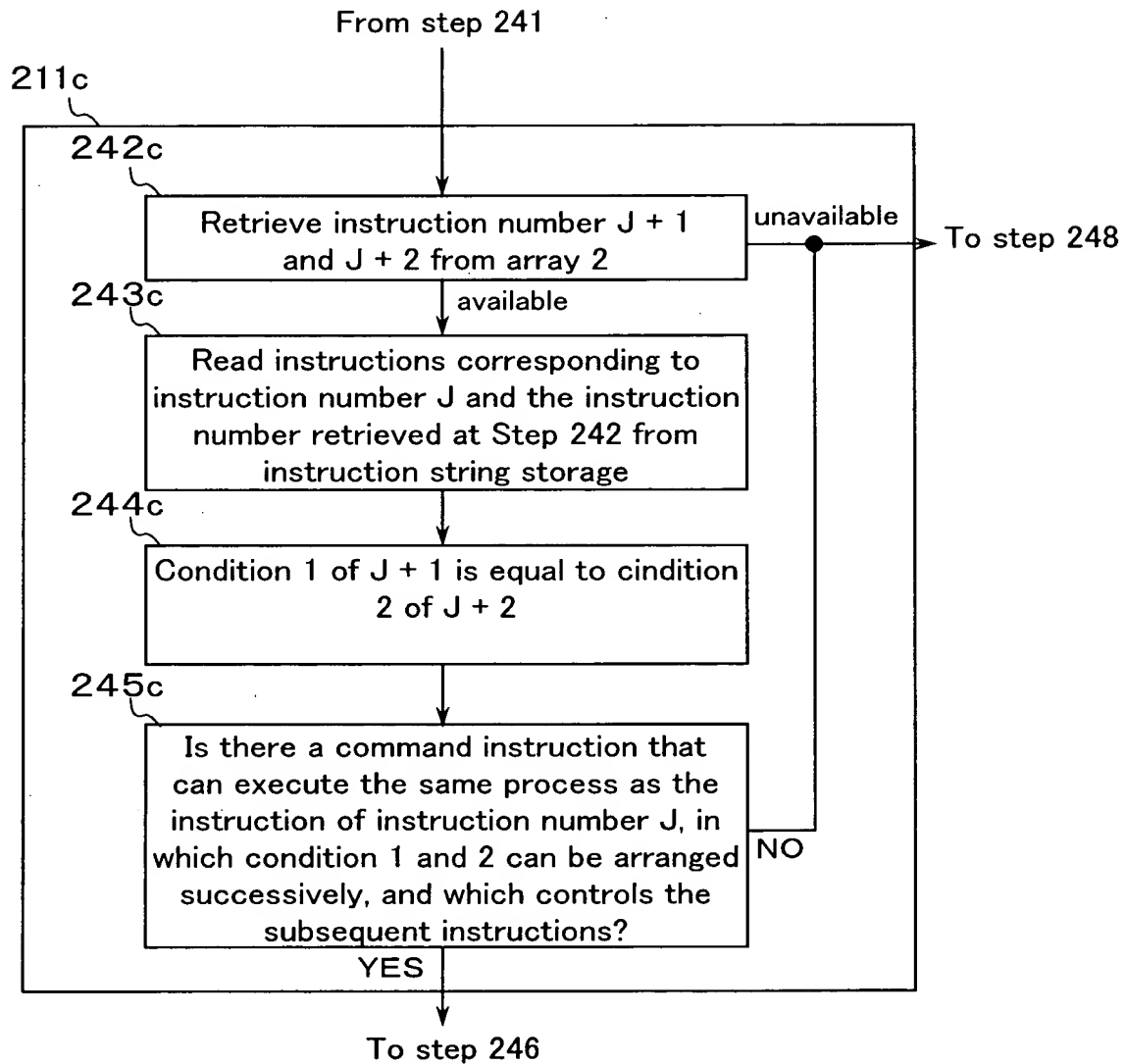


FIG. 27

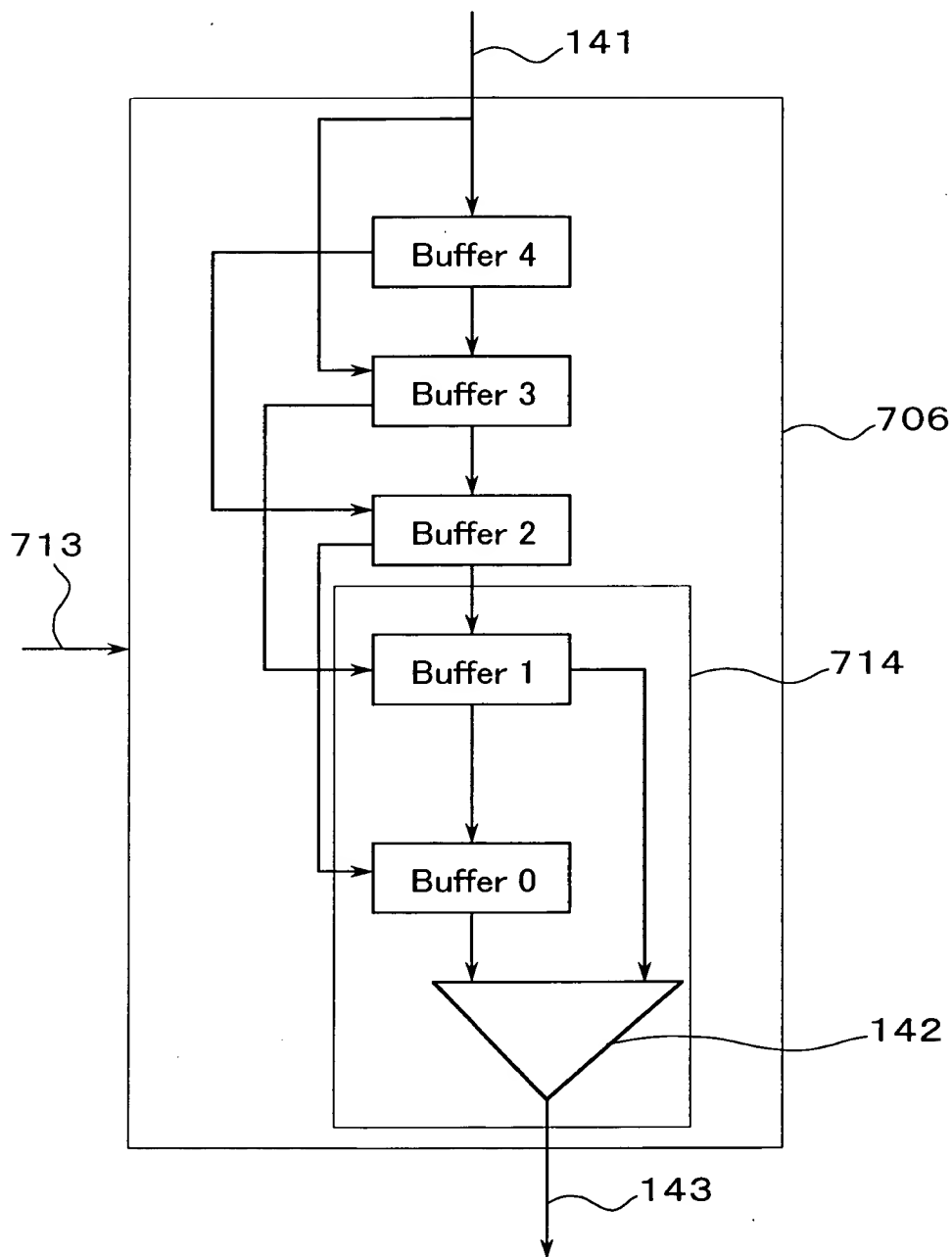


FIG. 28

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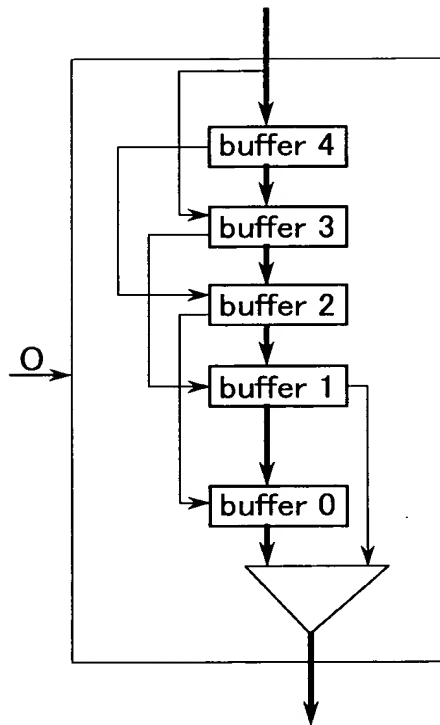


FIG. 29A

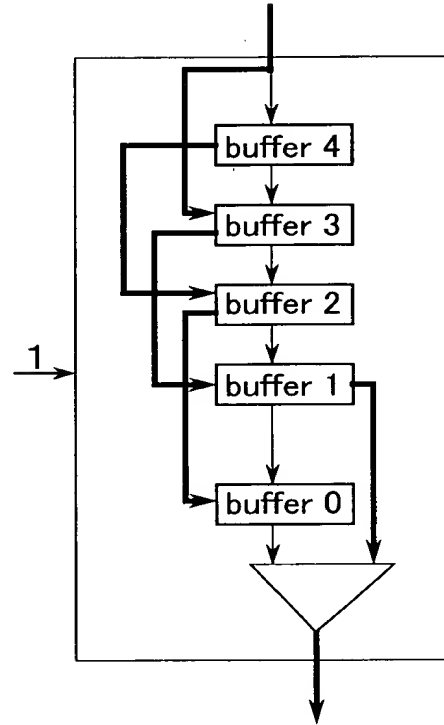


FIG. 29B

Conditional execution status Exclusive condition	x'00	x'01	x'10	x'11
1	Instruction overriding signal "0"	×	Instruction overriding signal "0"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 30A

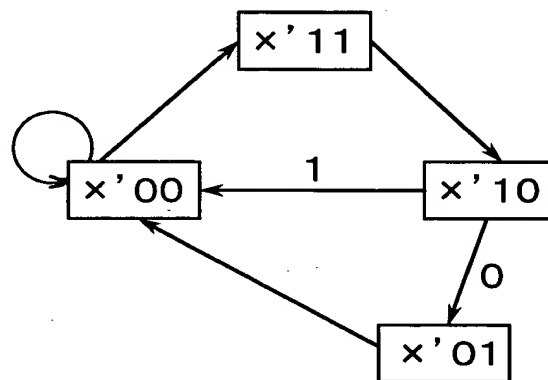


FIG. 30B

Conditional execution status Exclusive condition	x'00	x'01	x'10	x'11
1	0	0	1	0
0	0	0	0	0

FIG. 30C

108290" 50246860

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Buffer 4	Instruction 5	Instruction 6	Instruction 7	—	—
Buffer 3	Instruction 4	Instruction 5	Instruction 6	Instruction 8	Instruction 9
Buffer 2	Instruction 3	Instruction 4	Instruction 5	Instruction 7	Instruction 8
Buffer 1	Instruction 2	Instruction 3	Instruction 4	Instruction 6	Instruction 7
Buffer 0	Instruction 1	Instruction 2	Instruction 3	Instruction 5	Instruction 6

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 5	Instruction 6
DEC stage	Instruction 1		Instruction 2	Instruction 4	Instruction 5
EX stage			Instruction 1	Instruction 2	Instruction 4

Conditional execution status	x'00	x'00	x'11	x'10	x'00	x'00
Instruction prefetch control signal	0	0	0	1	0	0
Exclusive condition	0	0	0	1	1	1
Instruction overriding signal	0	0	0	0	0	0
	t1	t2	t3	t4	t5	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	

FIG. 31

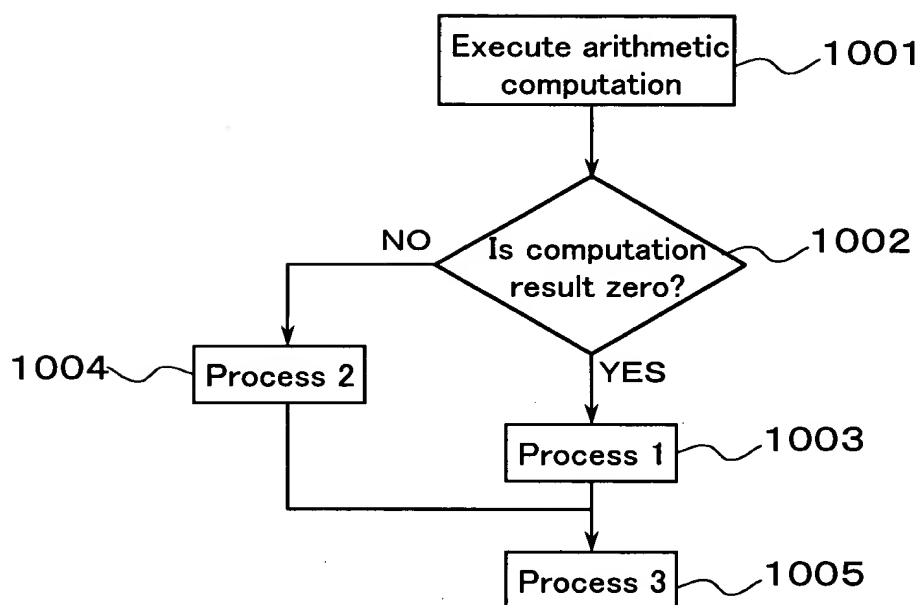


FIG. 32  
(PRIOR ART)

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108290-50246860

First line	SUB R0,R1
Second line	BNE label 1
Third line	Instruction 1
Fourth line	JMP label 2
Fifth line	label 1: Instruction 2
Sixth line	label 2: Instruction 3

FIG. 33  
(PRIOR ART)

09894205-1062801

First line	SUB R0,R1
Second line	MOVIFZF R2,R4
Third line	MOVIFNZF R3,R4
Fourth line	ADD R5,R6

FIG. 34  
(PRIOR ART)

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T08290-50246860



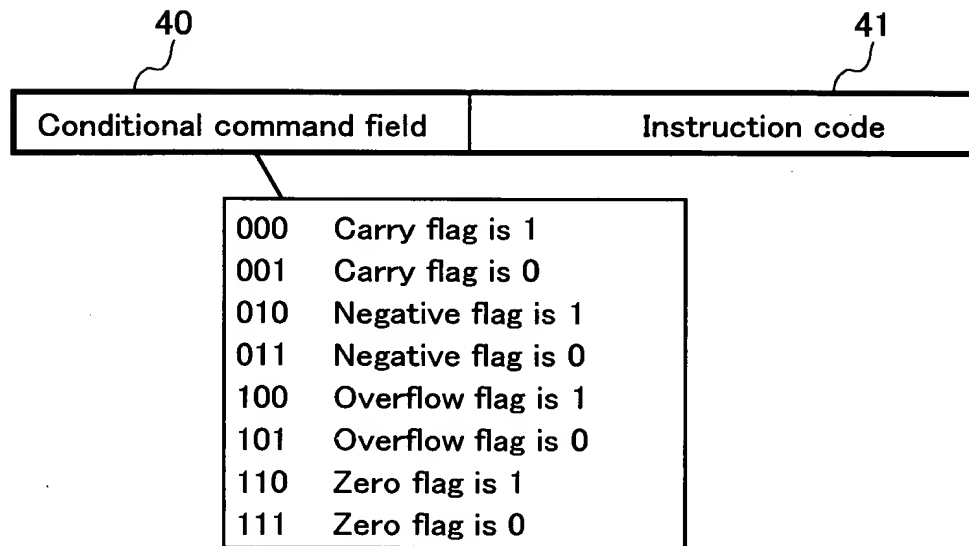


FIG. 35  
(PRIOR ART)

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